IN THE CLAIMS

Please amend the claims as follows:

Claims 1-8 (Canceled).

Claim 9 (Currently Amended): A wide-band amplifier comprising:

an input terminal configured to receive an input voltage;

an output terminal configured to provide an amplified output voltage;

an amplification device connected between the input terminal and the output terminal, an output of the amplification device being directly connected to the output terminal;

an LC parallel resonant circuit connected between the output terminal and a ground terminal in parallel to the amplification device; and

an LCR series resonant circuit connected between the output terminal and the ground terminal in parallel to the amplification device and the LC parallel resonant circuit,

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 10 (Previously Presented): An amplifier according to claim 9, wherein the amplification device includes a combination of a common-gate circuit and a cascade circuit.

Claim 11 (Previously Presented): An amplifier according to claim 9, wherein the amplification device includes a combination of a common-source circuit, a cascade circuit, and a voltage feedback circuit.

Claim 12 (Currently Amended): A wireless communication apparatus comprising:

an antenna;

a band-pass filter;

a low noise amplifier configured to amplify a voltage of a received signal, the low noise amplifier including

an input terminal configured to receive the received signal;

an output terminal configured to provide an amplified signal;

an amplification device connected between the input terminal and the output terminal, an output of the amplification device being directly connected to the output terminal of the low noise amplifier,

an LC parallel resonant circuit connected between the output terminal and a ground terminal in parallel to the amplification device, and

an LCR series resonant circuit connected between the output terminal and the ground terminal in parallel to the amplification device and the LC parallel resonant circuit;

a down-converter connected to the output terminal of the low noise amplifier and configured to down-convert the amplified signal provided by the output terminal by frequency conversion;

an automatic gain controller;

an analog-digital converter; and

a signal processing circuit configured to perform digital signal processing of received data,

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 13 (Currently Amended): A wireless communication apparatus comprising:

an antenna;

a band-pass filter;

a low noise amplifier configured to amplify a voltage of a received signal, the low noise amplified including

an input terminal configured to receive the received signal;

an output terminal configured to provide an amplified signal;

an amplification device connected between the input terminal and the output terminal,

an LC parallel resonant circuit connected between the output terminal and a ground terminal in parallel to the amplification device, and

an LCR series resonant circuit connected between the output terminal and the ground terminal in parallel to the amplification device and the LC parallel resonant circuit;

a down-converter connected to the output terminal of the low noise amplifier and configured to down-convert the amplified signal provided by the output terminal by frequency conversion;

an automatic gain controller;

an analog-digital converter;

a digital-analog converter configured to convert transmit data to an analog signal, the down-converter being directly coupled to the amplification device;

an up-converter configured to up-convert the analog transmit signal by frequency conversion;

a power amplifier configured to amplify a power of the up-converted transmit signal; and

a signal processing circuit configured to perform digital signal processing of transmit/receive data,

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 14 (Currently Amended): A wide-band amplifier comprising:

an input terminal configured to receive an input voltage;

an output terminal configured to provide an output voltage;

an amplification device connected between the input terminal and the output terminal, and output of the amplification device being directly connected to the output terminal; and

an analog band-pass filter connected between the output terminal and a ground terminal in parallel to the amplification device, the analog band-pass filter having a plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the s-plane,

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 15 (Previously Presented): An amplifier according to claim 14, wherein the band-pass filter does not have a capacitor provided in series with an output terminal of the amplifier.

Claim 16 (Previously Presented): An amplifier according to claim 14, wherein an inductance and a capacitor are not provided in series between an output terminal of the amplification device and an output terminal of the amplifier.

Claim 17 (Previously Presented): An amplifier according to claim 14, wherein the amplification device includes a combination of a common-gate circuit and a cascade circuit.

Claim 18 (Previously Presented): An amplifier according to claim 14, wherein the amplification device includes a combination of a common-source circuit, a cascade circuit, and a voltage feedback circuit.

Claim 19 (Currently Amended): A wireless communication apparatus comprising:

an antenna;

a band-pass filter;

a low noise amplifier configured to amplify a voltage of a received signal, the low noise amplifier including

an input terminal to receive the received signal;

an output terminal to provide an amplified signal;

an amplification device connected between the input terminal and the output terminal, an output of the amplification device being directly connected to the output terminal, and

an analog band-pass filter connected between the output terminal and a ground terminal in parallel to the output terminal of the amplification device, the analog band-pass filter having a plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the s-plane;

a down-converter connected to the output terminal and configured to down-convert the amplified signal provided by the output terminal by frequency conversion;

an automatic gain controller;

an analog-digital converter; and

a signal processing circuit configured to perform digital signal processing of received data.

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 20 (Currently Amended): A wireless communication apparatus comprising:

an antenna;

a band-pass filter;

a low noise amplifier configured to amplify a voltage of a received signal, the low noise amplifier including

an input terminal configured to receive the received signal;

an output terminal configured to provide an amplified signal;

an amplification device connected between the input terminal and the output terminal, an output of the amplification device being directly connected to the output terminal, and

an analog band-pass filter connected between the output terminal and a ground terminal in parallel to the output terminal of the amplification device, the analog band-pass filter having a plurality of poles provided on a left side of an s-plane and a plurality of zeros arranged between the poles, at least two zeros being arranged at locations other than an origin of the s-plane;

a down-converter connected to the output terminal and configured to down-convert the amplified signal by frequency conversion;

an automatic gain controller;

an analog-digital converter;

a digital-analog converter configured to convert transmit data to an analog signal;

an up-converter configured to up-convert the analog transmit signal by frequency conversion;

a power amplifier configured to amplify a power of the up-converted transmit signal; and

a signal processing circuit configured to perform digital signal processing of transmit/receive data,

wherein the amplification device includes a first MOS-FET transistor having a drain connected to a source of a second MOS-FET transistor, a drain of the second MOS-FET transistor being connected to the output terminal, a source of the first MOS-FET transistor being connected to the input terminal, a gate of the first MOS-FET transistor being connected to a first bias terminal via a bias resistor and to the ground terminal via a first bias capacitor, the gate of the second MOS-FET transistor being connected to a second bias terminal and to the ground terminal via a second bias capacitor.

Claim 21 (Cancelled)